1500V MOS Gated Thyristor

Symbol | Test Conditions | Maximum Ratings
--- | --- | ---
V<sub>DM</sub> | TJ = 25°C to 150°C | 1500 V
V<sub>GK</sub> | Continuous | ±30 V
V<sub>GK</sub> | Transient | ±40 V
I<sub>TSM</sub> | TC = 25°C, 1μs | 15.5 kA
TC = 25°C, 10μs | 6.4 kA
P<sub>D</sub> | TC = 25°C | 320 W
T<sub>J</sub> | -55 ... +150 °C
T<sub>DM</sub> | 150 °C
T<sub>Stg</sub> | -55 ... +150 °C
T<sub>L</sub> | Maximum Lead Temperature for Soldering | 300 °C
T<sub>SOLD</sub> | 1.6 mm (0.062 in.) from Case for 10s | 260 °C
V<sub>ISOL</sub> | 50/60Hz, 1 minute | 2500 V~
F<sub>C</sub> | Mounting Force | 50..200/11..45 N/lb
Weight | | 5 g

Features
* Silicon Chip on Direct-Copper Bond (DCB) Substrate
* Isolated Mounting Surface
* 2500V~ Electrical Isolation
* Very High Current Capability

Advantages
* High Power Density
* Low Gate Drive Requirement

Applications
* Capacitive Discharge Circuits
* Ignition Circuits
* Solid State Surge Protection

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<table>
<thead>
<tr>
<th>Symbol Test Conditions</th>
<th>Characteristic Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_ks</td>
<td>2825 pF</td>
</tr>
<tr>
<td>C_ogks</td>
<td>164 pF</td>
</tr>
<tr>
<td>C_og</td>
<td>50 pF</td>
</tr>
<tr>
<td>Q_g(on)</td>
<td>99 nC</td>
</tr>
<tr>
<td>Q_gk</td>
<td>22 nC</td>
</tr>
<tr>
<td>Q_ga</td>
<td>36 nC</td>
</tr>
<tr>
<td>t_h</td>
<td>Capacitive Discharge, T_J = 25°C</td>
</tr>
<tr>
<td>t_d</td>
<td>50 ns</td>
</tr>
<tr>
<td>t_h</td>
<td>Capacitive Discharge, T_J = 125°C</td>
</tr>
<tr>
<td>t_d</td>
<td>50 ns</td>
</tr>
<tr>
<td>R_thJC</td>
<td>0.39 °C/W</td>
</tr>
<tr>
<td>R_HCS</td>
<td>0.12 °C/W</td>
</tr>
<tr>
<td>R_thJA</td>
<td>30 °C/W</td>
</tr>
</tbody>
</table>

Notes:
1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. It is recommended to use a gate driver capable of supplying more than 4Amps and ≥15V gate voltage.
3. Refer to fig. 8 & 9.
Fig. 7. Cauer Thermal Network

\[
\begin{array}{c|c|c}
1 & 0.014083 & 0.0078555 \\
2 & 0.068078 & 0.0196550 \\
3 & 0.133430 & 0.1199600 \\
4 & 0.121939 & 2.5000000 \\
\end{array}
\]

Fig. 8. Capacitive Discharge

Fig. 9. Capacitive Discharge Waveform
NOTE:
1. ALL LEADS ARE MATTE PURE TIN PLATED.
2. CU SURFACE OF BOTTOM DCB IS PRE-NI PLATED UNLESS OTHERWISE.
3. CU SURFACE OF BOTTOM DCB IS ELECTRICALLY ISOLATED 2500V AC FROM ALL OTHER LEADS.
4. UNLESS OTHER SPECIFIED, PIN OUT ARE AS FOLLOWS.
   PINS:
   1 - GATE
   3 - Ks = Cathode Sense
   4 - 8 - K = Cathode
   9 - 16 - A = Anode